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All Silicon Electrode Photocapacitor for Integrated Energy Storage and Conversion

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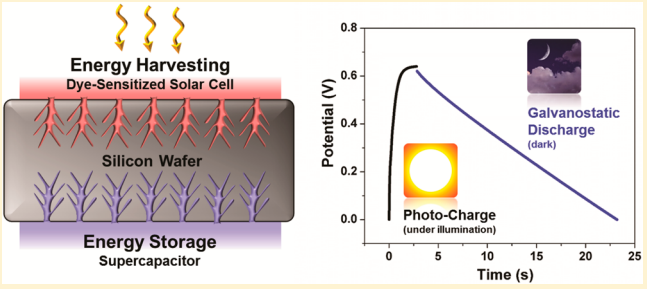
Supporting Information

ABSTRACT: We demonstrate a simple wafer-scale process by which an individual silicon wafer can be processed into a multifunctional platform where one side is adapted to replace platinum and enable triiodide reduction in a dye-sensitized solar cell and the other side provides on-board charge storage as an electrochemical supercapacitor. This builds upon electrochemical fabrication of dual-sided porous silicon and subsequent carbon surface passivation for silicon electrochemical stability. The utilization of this silicon multifunctional platform as a combined energy storage and conversion system yields a total device efficiency of 2.1%, where the high frequency discharge capability of the integrated supercapacitor gives promise for dynamic load-leveling operations to overcome current and voltage fluctuations during solar energy harvesting.



KEYWORDS: *Solar supercapacitor, photocapacitor, energy storage, dye-sensitized solar cell, supercapacitor, porous silicon, polymer electrolytes*

A key obstacle facing the practical incorporation of renewable energy technologies onto the power grid is the intermittent nature of renewable energy resources. The route toward decentralized energy systems that can produce an on-demand power output under intermittent cycles of power generation requires innovation in the devices and power electronics utilized for conversion systems. In this manner, integrating energy storage devices with energy harvesting technologies can provide the temporal flexibility needed to balance local power generation and power consumption.[1,2]

Among the various energy storage technologies, supercapacitors stand out with their capability to perform high-frequency cycling and high-power delivery while maintaining high round-trip efficiencies, which is necessary to sustain power quality management for grid-level applications.[3] Furthermore, storing charge through a physical double layer alleviates the issue of cycle-to-cycle fading and, as a result, commercial supercapacitors are rated for over a million cycles.[4] Additionally, unlike stationary power sources, such as lead-acid batteries, which are heavy and contain toxic or flammable materials that require external packaging, supercapacitors are a promising option for direct integration at the point of conversion. Such integration into the conversion materials themselves can eliminate additional ac−dc inversion, which improves the total energy efficiency of a power delivery unit installed in a home or building.

While the photocapacitor, a device that combines the function of energy conversion and energy storage, dates back a decade,[5] it has only been recently that such devices have been reported with practical efficiencies.[5−22] Furthermore, most devices that integrate energy storage and energy conversion into a single template require multistep fabrication techniques with nanocarbon materials and/or nanoscale metal-oxides that further strains the commercial outlook of the (typically) third-generation solar devices with which they are coupled, because the combined efficiency, manufacturing costs, and raw materials costs are the deciding factor for grid-scale deployment. In these reports, the best efficiencies reported for the combined storage and conversion system remain near or below 2%.[9] However, to qualify the integration route as being meaningful, any combined system must emphasize a cost, efficiency, or manufacturing benefit of integration versus the utilization of separate embodiments of energy storage and conversion. This specifically poses a challenge for devices requiring multiple sophisticated steps for material and device fabrication, devices relying on expensive materials, and devices where complex packaging requirements are necessary due to on-board electrolytes.

In this report, we overcome many of these challenges by using a simple, wafer-scale process to fabricate a multifunctional electrode from a silicon wafer. This central electrode replaces the Pt conventionally used in DSSC anodes while dually serving

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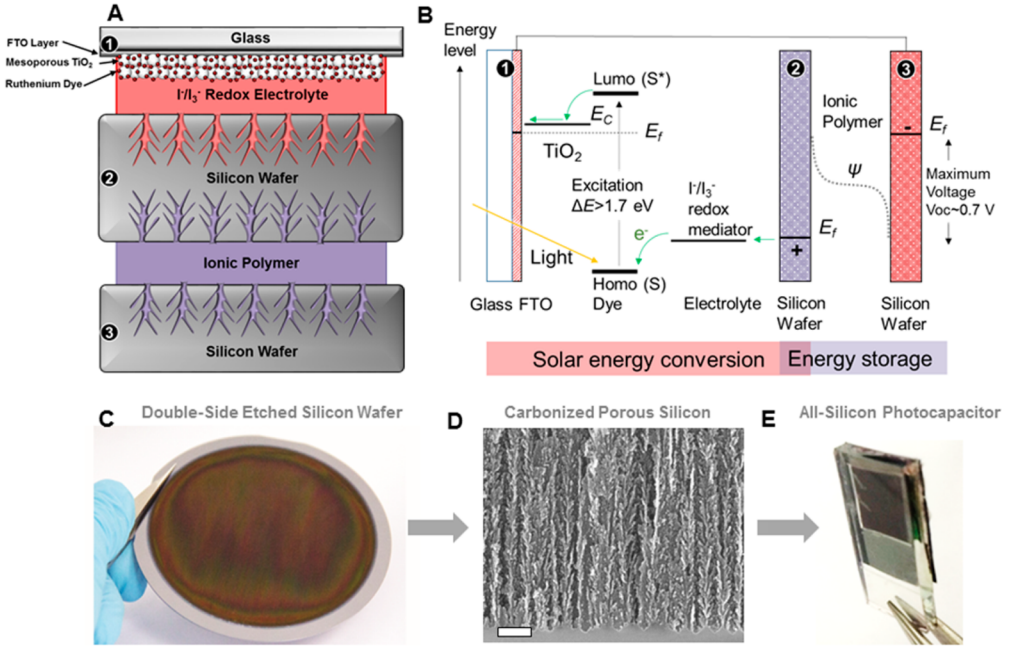

Figure 1. (A) Scheme of the integrated device configuration, showing the three-electrode architecture utilized in testing of the integrated, solid-state DSSC-supercapacitor system with SEM images of the porous silicon layer responsible for both the energy storage and conversion active materials in this device. (B) Band diagram of the photocapacitor device and charge transport processes occurring under illumination. (C) Photograph of a full 4″ silicon wafer following electrochemical etching. (D) SEM image of carbonized porous silicon material (SB = 200 nm). (E) Photograph of a representative full solid-state integrated DSSC-supercapacitor device as is utilized for the experiments in this work.

as an electrode for an electrochemical supercapacitor. Compared to other routes, where nanomaterial synthesis or fabrication must be employed on a common conductive electrode, our approach takes advantage of standard semiconductor manufacturing processes to utilize the material contained in a single silicon wafer for both energy storage and conversion functions. Capitalizing on common materials and techniques that benefit the performance of both functions, we demonstrate operation of this combined system with efficiency of up to 2.1%, which resides among the best values so far reported in the literature.

In order to transform a silicon wafer into a multifunctional electrode, we employ a two-step material fabrication process that involves (i) double-sided electrochemical fabrication of porous silicon, and (ii) a thermal carbon passivation that is self-catalyzed by the porous silicon material. Our device architecture, utilizing this central silicon wafer, is illustrated in Figure 1. The double-sided porous silicon etching is performed in an AMMT wafer-scale silicon etching system, where both sides of the electrode (0.01−0.02 Ωcm; p-Si) are exposed to an electrolyte containing 3:8 v/v HF and ethanol. Etching is performed equivalently on both sides of the silicon wafer to create an 8 μm deep nanoporous layer. The porous region consists of main pore channels that branch off into smaller subchannels resulting in a high-surface-area interface that is favorable for both charge storage and transfer (Figure 1D) with average pore size of ∼25 nm. Whereas silicon exhibits native reactivity with most electrochemical environments, our previous work has demonstrated that nanoscale silicon catalyzes a few-layered carbon (graphene-like) coating when heated in a thermal environment with a carbon precursor, protecting the silicon from electrochemical corrosion.[23,24] This previously discussed approach is utilized in this work using a double-sided porous silicon material, where both sides of the silicon wafer are exposed simultaneously to the flow of precursor gases in a chemical vapor deposition system using a ratio of 1:40:100 $C_2H_2/H_2/Ar$, respectively, at temperature ramps of up to 750 °C. Transmission electron microscopy (TEM) energy dispersive X-ray (EDS) characterization indicates the conformal nature of the carbon coating (Supporting Information Figure S1). Cross-sectional and top-view Raman maps indicate the uniformity of the carbon coating on the porous silicon and the consistency of the carbon chemical properties emphasized by the ratio of the D and G peaks observed in the Raman spectra (Supporting Information Figures S3 and S4). In order to demonstrate the usability of the supercapacitor electrode, we also fabricated an identically etched, single-sided silicon wafer to serve as the supercapacitor counter electrode, or anode (electrode 3). The supercapacitor electrodes were coupled with an ionic polymer, poly(ethylene-oxide)/1-ethyl-3-methylimidazolium tetrafluoroborate (PEO-EMIBF4) with 1:3 mass ratio, to serve as the solid-state supercapacitor electrolyte while also providing mechanical support as has been previously reported.[25] Finally, we constructed the FTO glass/TiO_2 DSSC anode (electrode 1) and secured it to the middle silicon electrode (electrode 2), which serves as the DSSC cathode, using heated Surlyn. Subsequently, an I^-/I_3^- redox electrolyte was injected into the sealed interface.[26] Further experimental details of material and device fabrication are available in the Supporting Information, including analysis of the TiO_2 electrode material (Supporting Information Figure S5). The fabrication process described yielded a self-supporting integrated energy storage and conversion device (Figure 1E) building upon active conversion and storage materials of TiO_2, Si, and C.

To clarify the operating mechanisms of the photocapacitor, Figure 1B illustrates the charge transport processes, and this is further discussed in detail in the Supporting Information

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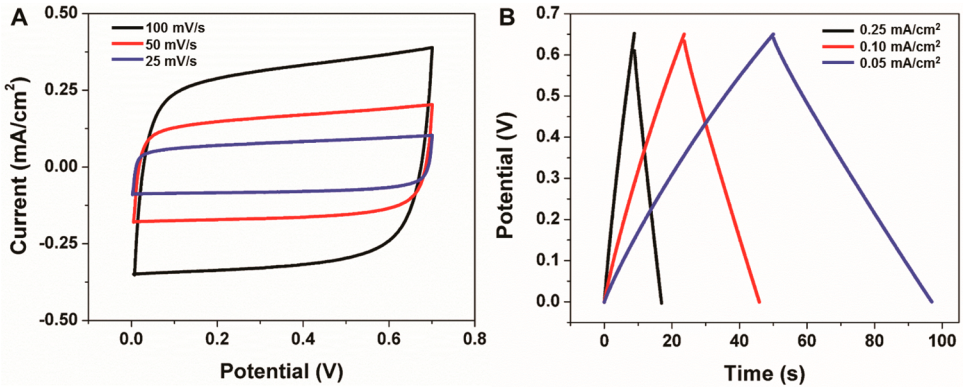

Figure 2. Analysis of the isolated supercapacitor performance in the integrated DSSC-supercapacitor. (A) Cyclic voltammetry curves at 25, 50, and 100 mV/s scan rates. (B) Galvanostatic charge−discharge curves taken at footprint-specific current densities of 0.05, 0.1, and 0.25 mA/cm^2.

(Figure S8). At the onset of charging, there is no potential difference between electrodes 1, 2, and 3. Photons from the incident solar illumination with energy greater than ∼1.7 eV are absorbed by the ruthenium dye, exciting dye molecules from the ground state (S) to the excited state (S*). Excited electrons from the dye are then injected into the conduction band of the TiO_2, resulting in the reduction of the dye (S^+). The injected electrons diffuse through the mesoporous TiO_2 layer to the FTO layer, which serves as the negative electrode (electrode 1). Electrons then travel through the external wiring to electrode 3, where they are stored in conjunction with the formation of an electrostatic double layer of mostly cations (EMI^+) in the ionic polymer. Meanwhile, the electrons that were lost by the dye are replenished by the iodine redox mediator that reduces the S^+ dye back to its ground state (S). In this process, the iodine ions (I^-) are oxidized to form I_3^-, which diffuses to the carbonized porous silicon (electrode 2), where the carbon coating facilitates the reduction back to iodine ions (I^-). The continued oxidation of the iodine redox mediator drains electrons from electrode 2, giving it a net positive charge and driving the formation of an electrostatic double layer of mostly anions (BF_4^-) in the ionic polymer on the "supercap side" of electrode 2. These double layers that form simultaneously at the electrode−ionic polymer interface of the high-surface area electrodes (2 and 3) facilitate the efficient storage of the photogenerated charge. The photocurrent will continue to bring electrons from electrode 2 to electrode 3, by way of electrode 1, until a voltage equal to the V_{OC} (∼0.7 V) is built up at which point the oxidized dye (S^+) will cease to be reduced back to its ground state (S) and the net current flow in the device will drop to zero. It should be noted in this case that the purpose of the carbon layer on the surface of the porous silicon is to act as a passive electrochemical interface that reverses the compromised electrical properties of highly doped porous silicon due to surface defects.[24]

In order to assess the combined integrated device performance, we first examined the individual performance of the electrochemical supercapacitor and the DSSC in the integrated system. This was performed by electrically isolating the individual supercapacitor electrodes (2 and 3) and the DSSC electrodes (1 and 2) as labeled in Figure 1. In this manner, we assessed the integrated supercapacitor through electrochemical analysis including cyclic voltammetry and galvanostatic charge−discharge measurements, shown in Figure 2. As the supercapacitor operating voltage for the integrated device only extends through the voltage range defined by the open-circuit voltage (V_{OC}) of the DSSC, we performed measurements only up to 0.65−0.7 V. This is well within the range of the supercapacitor electrochemical window, and CV scans at three rates of 100, 50, and 25 mV/s (Figure 2A) demonstrate a near-ideal boxlike shape of the CV curves indicating low internal resistance and stable charge storage in this operating range. Galvanostatic charge−discharge measurements (Figure 2B) were performed at currents normalized to the footprint specific area of the device, which is most relevant for planar integration, which extended from 0.05 to 0.25 mA/cm^2. The nearly perfect triangular shape of the charge−discharge curves indicates an ideal supercapacitor charge storage mechanism in this voltage range with good Coulombic efficiency. Specifically, at slow charging rates of 0.1 mA/cm^2, we measure a Coulombic efficiency of 94% and an overall energy efficiency of 80% with a footprint-specific capacitance measured to be 3.5 mF/cm^2 (∼5.7 C/g based on the active tethered porous silicon material) and a footprint equivalent series resistance of 84 Ω·cm^2. This non-Faradaic charge storage performance is improved in comparison to other recent reports using materials such as TiO_2 nanotubes and ZnO nanowires.[20,22]

In order to assess the performance of only the DSSC component of the integrated system, we performed $I-V$ scans (Figure 3). From this $I-V$ curve assessment, we measured a short circuit current density (J_{SC}) of 11.5 mA/cm^2, a V_{OC} of

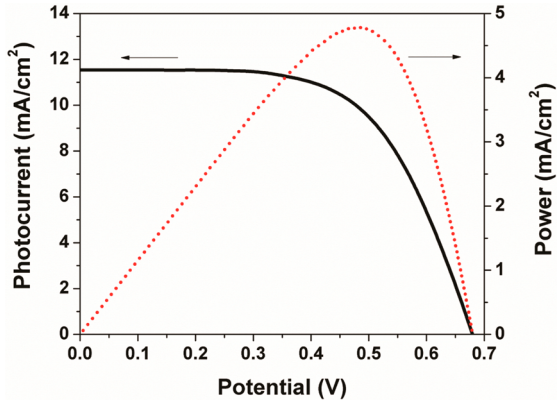

Figure 3. Assessment of the isolated DSSC performance in the integrated DSSC-supercapacitor system, specifically showing the $I-V$ curve profile (black) and the voltage-power efficiency profile emphasizing the maximum power point near 0.49 V, consistent with this DSSC system.

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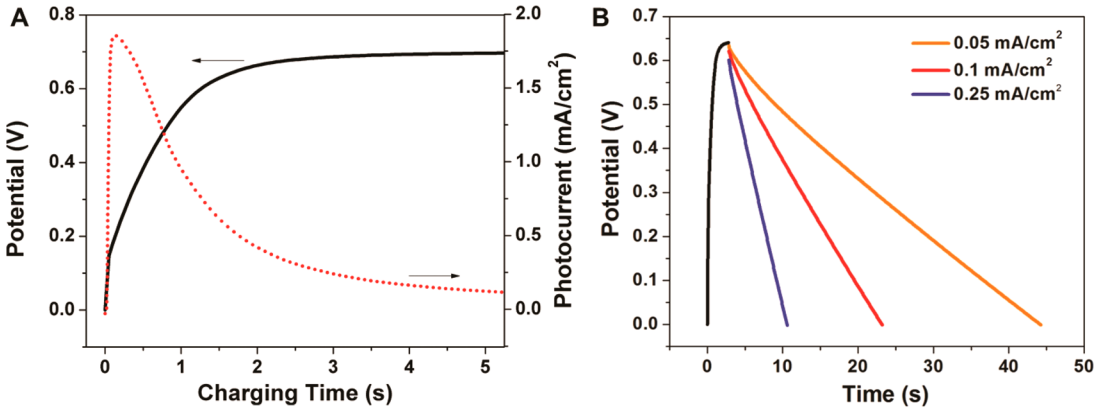

Figure 4. Device characterization of the full, integrated silicon DSSC-supercapacitor device. (A) Voltage as a function of time for photocharging of an integrated system using the DSSC; the corresponding current−time profile is shown in red, emphasizing that the majority of stored charge occurs at voltages below 0.6 V. (B) Light-charging and dark-discharging curves relative to supercapacitor footprint showing photocharging to 0.64 V, and subsequent dark Galvanostatic supercapacitor discharging at rates of 0.05, 0.1, and 0.25 mA/cm^2. Additional data for discharging rates of 0.01 mA/cm^2 are shown in the Supporting Information, emphasizing discharging times up to 200 s.

0.68 V, and a fill factor of 61%, which are comparable to literature values for DSSCs. At the maximum power point of 0.49 V, the DSSC demonstrated 4.8% power conversion efficiency, though this power conversion efficiency does not directly correlate to the integrated device efficiency because charge storage occurs over a range of voltages and power conversion efficiencies drop from this value on either side of the maximum power point.

Following device testing of the individual DSSC and supercapacitor components, we tested the integrated device using a manual illumination-dark state process: (i) the device was charged using AM 1.5G illumination (100 mW/cm^2) from a Newport solar simulator until reaching a set cutoff voltage near the V_{OC} and (ii) the illumination was blocked, the electrical connection between electrodes 1 and 3 was removed, and the device was galvanostatically discharged in the dark. This testing method is discussed in greater detail in the Supporting Information. The temporal charging profile (Figure 4) demonstrates both the dynamic change in photocurrent and voltage as a function of charging time, where the photocurrent is measured across the DSSC and supercapacitor (electrodes 1 and 3), and the voltage is measured across the supercapacitor (electrodes 2 and 3). Evident from this plot, the voltage profile of the supercapacitor exhibits a plateau near the V_{OC} of the DSSC with the majority of the photocurrent stored at voltages below 0.6 V.

In order to demonstrate the combined function of the device, emphasizing the ability of the integrated system to harvest solar energy and deliver that energy under dark conditions (e.g., when a cloud passes overhead, or in the circumstance of a power spike), we demonstrate the ability to photocharge the integrated system using the above-mentioned setup, and galvanostatically discharge the device at currents of 0.05, 0.1, and 0.25 mA/cm^2 (Figure 4B) with a charging cutoff voltage of 0.64 V, near the V_{OC}. From the 0.1 mA/cm^2 discharge curve, we calculate the energy density and power density of the discharge to be 0.17 μWh/cm^2 and 22 μW/cm^2 respectively. The energy and power density for all of the discharging currents are reported in the Supporting Information. Furthermore, in order to demonstrate the device stability under extended cycling, we performed 10 repeated cycles of photocharging and galvanostatic discharging that is in accordance with the stable individual cycling and operation of the supercapacitor and DSSC components (Figures S9, S10, and S11 in Supporting Information).

Examining the DSSC power curve shown in Figure 3, it is clear that the solar conversion efficiency drops off as the operating voltage approaches the V_{OC}. Using this insight, which has been previously reported,[20] we limited the cutoff voltage of the photocapacitor to 0.6 V. As a result, the device was able to store 80% of the energy in a significantly shorter charging time (1.2 s rather than 2.8 s). In this manner, we were able to demonstrate an overall efficiency of 2.1% (Supporting Information Figure S6). Furthermore, due to the low equivalent series resistance (ESR) of the supercapacitor measured as 84 Ω·cm^2 from Figure 2B, high frequency power delivery can occur with negligible power loss, which complements energy harvesting systems prone to intermittent fluctuations based on environmental conditions.

Going forward from this proof-of-concept device architecture, we envision routes that can significantly improve the energy storage and power delivery capability of this device. First of all, our system utilizes a porous silicon energy storage material with depth of 8 μm. Previous studies have emphasized the capability to etch porous silicon to depths over 0.2 mm, which we anticipate will significantly increase the total footprint energy storage capability of these systems.[27,28] Additionally, the use of architectures to improve voltage and cell-level usability, such as tandem DSSC systems, can improve the V_{OC} and maximum power voltage profile of the DSSC, better utilizing the large electrochemical window of the supercapacitor. Because the total energy stored in an ideal supercapacitor scales as $E = 1/2CV^2$, where V is the voltage at which the charge is stored, doubling the voltage in a tandem cell improves the energy stored by four times, for example. Beyond this, we envision routes where multiple devices are connected into full-size panels using ion conducting backplanes to store charge between devices and deliver voltages compatible with household or grid applications. Such devices could be important to enable constant power delivery in microgrid systems as well as for power balancing during energy conversion.

In summary, we demonstrate the ability to produce a photocapacitor where an individual silicon wafer can be processed as a multifunctional energy storage and conversion unit using a straightforward fabrication route that builds upon conventional wafer-scale silicon semiconductor manufacturing

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processes. This enables a silicon wafer to simultaneously perform the Faradaic charge transfer role of a DSSC as well as the non-Faradaic double-layer charge storage role of an electrochemical supercapacitor. Unlike other routes for integration, where individual materials are combined into a heterogeneous electrode, usually involving Pt and other conductive nanomaterials for DSSC-storage systems, our work adapts silicon to play both roles of energy storage and conversion, which eliminates the necessity for Pt in the DSSC and appeals to the true theme of integration. On a large scale, the development of integrated energy storage and conversion systems may be an enabling technology for the future of a decentralized energy grid and greater penetration of renewable energy resources into existing grids that have low tolerance to overcome the variability introduced by intermittent renewable power generation. Furthermore, the use of silicon to accomplish this builds upon global incentives that focus on the low-cost manufacturing of silicon materials for solar applications, where this device architecture combines silicon with other sustainable materials such as TiO_2 to produce efficient integrated solar-storage systems.

■ ASSOCIATED CONTENT

Supporting Information

Additional information and figures. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

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Author Contributions

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Notes

The authors declare no competing financial interest.

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