

Effects of anneals in ammonia on the interface trap density near the band edges in 4H–silicon carbide metal-oxide-semiconductor capacitors

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Results of room temperature capacitance–voltage measurements are reported for SiO₂/4H–SiC (*n* and *p* type) metal-oxide-semiconductor capacitors annealed in ammonia following oxide layer growth using standard wet oxidation techniques. For *n*-SiC capacitors, both the interface state density near the conduction band edge and the effective oxide charge are substantially reduced by the ammonia anneals. For 2 h anneals, the oxide charge appears to have a minimum value for an anneal temperature of approximately 1100 °C. However, for *p*-SiC, anneals in ammonia produce no improvement in the interface state density near the valence band edge, and the effective oxide charge is not reduced compared to samples that were not annealed. Results are compared to those reported previously for anneals in nitric oxide. Ion beam analyses of the oxide layers show substantially more nitrogen incorporation with the ammonia anneals, although for *n*-SiC, the decrease in D_{it} is comparable for both nitric oxide and ammonia anneals. Results reported here for ammonia and those reported previously for nitric oxide are the first to demonstrate that significant passivation of the interface state density near the conduction band edge in SiC can be achieved with high temperature anneals using either gas. This demonstration has important implications for SiC metal-oxide-semiconductor field effect transistor technology development. © 2000 American Institute of Physics. [S0003-6951(00)00948-7]

Silicon carbide has material properties that make it superior to Si for a number of electronic device applications.¹ Bulk SiC wafers are currently available in 5 cm diameters, and the community anticipates having 10 cm diameter wafers within the next few years. Defect densities have been reduced significantly over the past five years, and micropipe defect densities of less than 1 cm⁻³ have been demonstrated. Improvements in material quality support the development of silicon carbide electronic devices that will operate reliably in high power, high temperature, high frequency, and high radiation environments where Si devices will not operate.

Silicon carbide is the only wide band gap semiconductor that has a native oxide, and metal-oxide-semiconductor field effect transistors (MOSFETs) have been fabricated using both the 4H and 6H polytypes of SiC. The 4H polytype has higher, more isotropic bulk carrier mobilities,² and is hence the polytype of choice for MOSFET fabrication. However, as the result of a relatively high SiO₂/SiC interface state density (10¹³ cm⁻² compared to ~10¹⁰ cm⁻² for Si), 4H–SiC *n*-channel, inversion mode MOSFETs are characterized by very low (single digit) channel mobilities. Assuming an inversion channel depth of 10 nm and an inversion channel carrier concentration of 10¹⁹ cm⁻³ for two MOSFETs, one Si and one SiC, the channel carrier concentration during device

operation (i.e., in inversion) is approximately 10¹³ cm⁻² for both devices. Therefore it follows that, for any assumed trapping efficiency (1 carrier/trap, 0.5 carriers/trap, etc.), carrier trapping is a much more serious problem for SiC MOSFETs than for Si devices. Carrier trapping lowers channel mobility and results in a reduced current handling capability for the MOSFET.

Schorner *et al.*³ attribute the poorer performance of 4H devices to a large, broad interface state density located at approximately 2.9 eV above the valence band edge in both polytypes. For 6H–SiC ($E_{gap} \sim 3$ eV), these states lie mostly in the conduction band, and hence have little effect on inversion channel mobility. However, for 4H–SiC ($E_{gap} \sim 3.3$), the interface states lie mostly in the band gap where they act to reduce channel mobility through field termination, carrier trapping, and Coulomb scattering. Afanasev *et al.*⁴ have proposed that interface states in SiC/SiO₂ structures result from carbon clusters at the interface and defects in a near-interface suboxide that is produced when the oxidation process is terminated. The large interface trap density near the conduction band edge proposed by Schorner *et al.* has been observed experimentally,^{5–7} and much attention is currently given to finding methods of passivation for these states. Passivation techniques can be studied using *n*-SiC since the trap densities near the conduction band edge are similar for both *n*- and *p*-SiC.^{5,7} Channel mobility measurements for *n* channel, inversion mode devices will determine whether any passiva-

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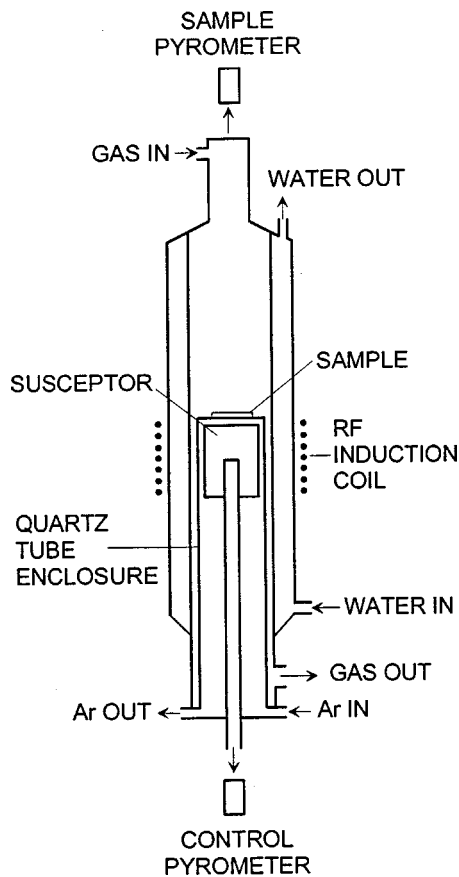


FIG. 1. Annealing furnace for postoxidation anneals in NH_3 . The SiC-coated graphite susceptor is heated by rf induction.

tion technique actually improves the device fabrication process.

Li *et al.*⁸ originally reported improvements in the electrical performance of dry oxides on 6H-SiC annealed in nitric oxide. We have recently annealed wet oxides in NO ⁹ and found that the interface state density near the conduction band edge in 4H-SiC can be reduced by factors of 4–5 to levels comparable to the interface state density near the conduction band edge in 6H-SiC. In this letter we report the results of annealing studies using ammonia. We also report measurements of nitrogen uptake in the NH_3 process and show that the incorporated nitrogen content is approximately two orders of magnitude greater compared to nitrogen incorporation from the NO process.

Five micron 4H-SiC epilayers (N_d and $N_a = 8 \times 10^{16}$ and $3 \times 10^{16} \text{ cm}^{-3}$, respectively) purchased from Cree Research, Inc. were oxidized using standard, wet oxidation techniques that have been described elsewhere.¹⁰ Following oxidation to produce 40 nm oxide layers, the samples were annealed in NH_3 using the furnace shown in Fig. 1. A vertical epitaxial growth reactor has been modified by enclosing the reactor's SiC-coated graphite susceptor in high purity quartz. An optical pyrometer is used to measure the temperature of samples that are placed on top of the quartz enclosure during the annealing process. The high purity quartz tube prevents contamination of the oxide layers by carbon that can escape from the susceptor at elevated temperatures. The furnace was evacuated and flushed with Ar several times, after which NH_3 was introduced at a pressure of 1 atm. The NH_3 flow rate was maintained at 0.5 l/min during the an-

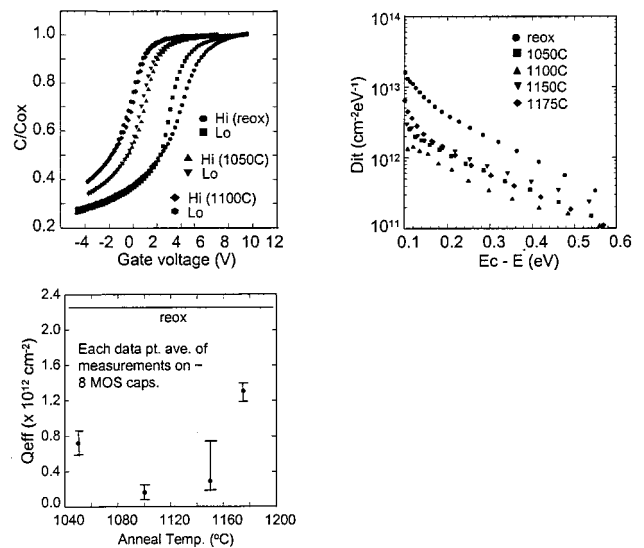


FIG. 2. Results for 2 h anneals of $\text{SiO}_2/n\text{-4H-SiC}$ samples in NH_3 —room temperature $C-V$ curves, interface state density D_{it} , and effective oxide charge Q_{eff} . The interface state density near the conduction band edge is reduced by almost one order of magnitude by the anneal in NH_3 .

nealing process. Each sample was annealed for 2 h in 1 atm of flowing ammonia at a temperature between 1050 and 1175 °C.

In a separate furnace, oxide layers (~ 12.5 nm) grown on 4H-SiC were annealed in flowing NH_3 for subsequent measurements of nitrogen content. Rutherford backscattering/channeling was used to determine the nitrogen accumulation as a function of temperature.

The results of room temperature $C-V$ measurements are shown in Figs. 2 and 3 for $n\text{-4H-SiC}$ and $p\text{-4H-SiC}$, respectively. In these figures, “re-ox only” refers to samples that were not annealed in NH_3 . Our standard oxidation process is terminated with a “reoxidation” step that is carried out at several hundred degrees below the oxidation temperature of 1100 °C. The reoxidation process improves the inter-

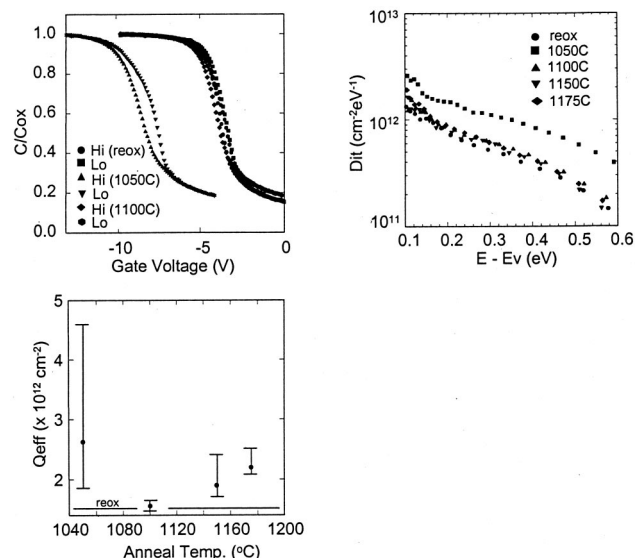


FIG. 3. Results for 2 h anneals of $\text{SiO}_2/p\text{-4H-SiC}$ samples in NH_3 —room temperature $C-V$ curves, interface state density D_{it} , and effective oxide charge Q_{eff} . Compared to samples that were not annealed (reox), no improvement is observed for the interface state density in the lower half of the band gap near the valence band edge.

face state density near midgap for *p*-SiC/SiO₂ MOS capacitors.^{5,11,12} For *n*-SiC (Fig. 2), significant improvements have been achieved compared to samples that were not annealed. Both the interface state density D_{it} near the conduction band edge and the effective oxide charge Q_{eff} are substantially reduced by the anneals in NH₃, and both appear to have minimum values for an annealing temperature of about 1100 °C. Compared to results reported previously for nitric oxide,⁹ the effective oxide charge is much lower for *n*-4H-SiC/SiO₂ samples annealed in ammonia.

In contrast (see Fig. 3), postoxidation anneals in ammonia do not improve Q_{eff} and D_{it} near the valence band edge for *p*-SiC. The effective oxide charge does appear to have a minimum value for an anneal temperature approximately 1100 °C; however, values for Q_{eff} are similar to those measured for *p*-SiC samples that were not annealed.

To elucidate this unusual temperature dependence for the NH₃ anneals and to better understand the differences between NO and NH₃ annealing, we have undertaken a series of measurements of nitrogen uptake for these different annealing ambients. As reported in Ref. 13, NO annealing results in the accumulation of small amounts of nitrogen ($<6 \times 10^{14} \text{ cm}^{-2}$), concentrated near the SiC/SiO₂ interface. Results for N accumulation in SiC/SiO₂ following NH₃ anneals have not been reported. However in Si/SiO₂, it is known that NH₃ annealing can result in very large accumulations of nitrogen, with a substantial fraction of the dielectric being nitride-like.¹⁴

The nitrogen content in NH₃ annealed oxides was measured using RBS/channeling, and the values obtained were typically around $1.5 \times 10^{16} \text{ cm}^{-2}$ for temperatures in the range of 1050–1150 °C. The N incorporation is accompanied by a significant loss of oxygen in the oxide film, so that the ratio of oxygen to nitrogen is approximately 1.5:1 in the 12.5 nm films. This amount of nitrogen is almost two orders of magnitude higher than that in NO annealed oxides on SiC ($\sim 10^{14} \text{ cm}^{-2}$).¹³ The work of Koba and Tressler¹⁴ for Si/SiO₂ MOS capacitors annealed in NH₃ suggests that the uptake of nitrogen is almost independent of oxide thickness. Therefore, we expect that the 40 nm MOS capacitor oxides are comprised of approximately 20% nitrogen-containing species. This large amount of nitrogen must be in the form of a complex oxynitride with modified electrical properties. Nevertheless, the reduction of D_{it} for *n*-4H-SiC is similar for NO and NH₃ anneals, while the reduction in Q_{eff} is greater for the NH₃ anneal. These results may be explained by the relative locations of the nitrogen and the oxide charges in the SiO₂ layer.

In Si/SiO₂, annealing in NH₃ incorporates nitrogen throughout the bulk of the oxide, with peaks at the surface and interface, and removes oxygen from the film.¹⁴ Nitric oxide anneals, however, incorporate nitrogen only in a narrow region at the interface.¹⁵ Similar results are obtained for SiC/SiO₂. Nitrogen is incorporated at the interface during an NO anneal¹³ and throughout the oxide layer (bulk and interface) during anneals in NH₃. Nitrogen from an NO anneal improves the interface quality by reducing D_{it} , but has less effect for the fixed charge away from the interface in the

bulk of the oxide. However, nitrogen from the NH₃ anneal reduces contributions to Q_{eff} from the bulk of the oxide in addition to passivating states at the SiC/SiO₂ interface.

In conclusion, ammonia has been shown to be an effective annealing ambient for the reduction of the effective oxide charge and the interface state density near the conduction band edge in *n*-4H-SiC/SiO₂ MOS capacitors. Compared to control samples that were not annealed, D_{it} was reduced from $\sim 7 \times 10^{12}$ to $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, while Q_{eff} was reduced by an order of magnitude from 2×10^{12} to $2 \times 10^{11} \text{ cm}^{-2}$. These results for $D_{it}(E_c)$ are similar to those reported previously for postoxidation anneals in nitric oxide.⁹ Ammonia anneals also incorporate an extensive amount of nitrogen throughout the oxide, resulting in lower fixed charge densities and lower Q_{eff} .

For MOS capacitors fabricated using *p*-4H-SiC, the interface state density and the effective oxide charge are not improved by anneals in NH₃. Two possibilities contribute to these observations. The interface state density near the valence band edge in unannealed samples may be as much as one order of magnitude lower ($\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$) compared to D_{it} near the conduction band edge.^{5,9} Therefore, the effects of passivation may not be as dramatic near the valence band edge. Also, as reported previously for postoxidation anneals using NO, nitrogen passivation can shift the energies of carbon cluster states near the conduction band edge to the lower half of the band gap, thereby contributing to an increase in the interface state density near the valence band edge for *p*-MOS capacitors annealed in either ammonia or nitric oxide.

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- ¹J. B. Casady and R. W. Johnson, *Solid-State Electron.* **39**, 1409 (1996).
- ²*EMIS Data Reviews Series*, edited by G. L. Harris (Short Run, Exeter, UK, 1995), Vol. 13.
- ³R. Schorner, P. Friedrichs, D. Peters, and D. Stephani, *IEEE Electron Device Lett.* **20**, 241 (1999).
- ⁴V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, *Phys. Status Solidi A* **162**, 321 (1997).
- ⁵G. Y. Chung, C. C. Tin, J. H. Won, and J. R. Williams, *Mater. Sci. Forum* **338–342**, 1097 (2000).
- ⁶M. K. Das, B. S. Um, and J. A. Cooper, Jr., *Mater. Sci. Forum* **338–342**, 1079 (2000).
- ⁷N. S. Saks, S. S. Mani, and A. K. Agarwal, *Mater. Sci. Forum* **338–342**, 1113 (2000).
- ⁸H. Li, S. Dimitrijević, H. B. Harrison, and D. Sweatman, *Appl. Phys. Lett.* **70**, 2028 (1997).
- ⁹G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, *Appl. Phys. Lett.* **76**, 1713 (2000).
- ¹⁰G. Y. Chung, C. C. Tin, J. H. Won, J. R. Williams, K. McDonald, R. A. Weller, S. T. Pantelides, and L. C. Feldman, *Proceedings of 2000 IEEE Aerospace Conference* **7**, 1001 (2000).
- ¹¹L. A. Lipkin and J. W. Palmour, *J. Electron. Mater.* **25**, 909 (1996).
- ¹²M. K. Das, J. A. Cooper, and M. R. Melloch, *J. Electron. Mater.* **27**, 353 (1998).
- ¹³K. McDonald, M. B. Haung, R. A. Weller, L. C. Feldman, J. R. Williams, F. C. Stedile, I. J. R. Baumvol, and C. Radtke, *Appl. Phys. Lett.* **76**, 568 (2000).
- ¹⁴R. Koba and R. E. Tressler, *J. Electrochem. Soc.* **135**, 144 (1988).
- ¹⁵I. J. R. Baumvol, *Surf. Sci. Rep.* **36**, 1 (1999).